Express Mail Label No. EL089369806US

02-24-00

A

jc571 U.S. PTO 02/23/00

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. 13392
Total Pages in this Submission 3

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

DEMODULATION AND MODULATION CIRCUIT AND DEMODULATION AND MODULATION METHOD

jc590 U.S. PTO 09/510861 02/23/00

and invented by:

Koichi Tamura

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 31 pages and including the following:
   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
13392
Total Pages in this Submission
3

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 12
   b. ☐ Informal Number of Sheets

4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing
   ☐ First Class ☒ Express Mail *(Specify Label No.):* EL089369806US

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
13392
Total Pages in this Submission
3

Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	28	- 20 =	8	x $18.00	$144.00
Indep. Claims	4	- 3 =	1	x $78.00	$78.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$690.00
OTHER FEE *(specify purpose)*		Assignment Recordal			$40.00
				TOTAL FILING FEE	$952.00

☒ A check in the amount of **$952.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **19-1013/SSMP** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: **February 23, 2000**

Paul J. Esatto, Jr.
Registration No. 30,749
SCULLY, SCOTT, MURPHY & PRESSER
400 Garden City Plaza
Garden City, New York 11530
516-742-4343

cc:

DEMODULATION AND MODULATION CIRCUIT AND DEMODULATION AND MODULATION METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to a demodulation and modulation circuit and demodulation and modulation method. More particularly, the invention relates to a demodulation and modulation circuit and demodulation and modulation method of a digital transmission signal to be used in a cellular phone terminal.

Description of the Related Art

Conventionally, sampling in an analog-to-digital (A/D) converter in a demodulation circuit causes phase shift due to a frequency offset between transmission and reception and thus cannot be performed constantly at optimal sampling timing.

Therefore, at certain sampling timing, it is possible to significantly degrade reception characteristics for occurrence of error in symbol judgment due to sampling of the reception signal close to zero crossing (boundary point in transition where symbol is changed from positive to negative or negative to positive).

The following equation shows adverse influence of the frequency offset for demodulation. It is assumed that a modulated wave is expressed by:

$$s(t) = A(t) \cos [2\pi fct + \phi(t)]$$

Here, A(t) is assumed to be +1 or -1, and a carrier wave component cos $[2\pi fct]$ of the modulated wave set forth above is a reference signal pi(t), an orthogonal demodulator output I component is expressed by:

$$I(t) = s(t) \times pi(t)$$
$$= A(t) \cos [2\pi fct + \phi(t)] \times \cos [2\pi fct]$$
$$= (A(t)/2) \times [\cos (4\pi fct + \phi(t)) + \cos \phi(t)]$$

By cutting off cos $(4\pi fct + \phi(t))$ as the second term on right side by LPF, the I component can be expressed by:

$$I(t) = (A(t)/2) \times \cos \phi(t)$$

to obtain phase information of I component of a PSK modulated wave.

Similarly, a carrier wave component -sin $[2\pi fct]$ which is obtained by shifting the phase for $\pi/2$ ahead of the modulated wave is a reference signal pq(t), an orthogonal demodulator output Q component is expressed by:

$$Q(t) = A(t) \cos [2\pi fct + \phi(t)] \times (-\sin [2\pi fct])$$

$$= A(t)/2) \times \cos \phi(t)$$

However, since the frequency offset $\Delta\theta(t)$ is caused between transmission and reception in the practical circuit, respective reference signals can be expressed by:

$$pi(t) = \cos [2\pi fct + \Delta\theta(t)]$$

$$pq(t) = -\sin [2\pi fct + \Delta\theta(t)]$$

The orthogonal demodulation output is expressed by multiplying the foregoing reference signal and the modulated wave and cutting off a high frequency component by the LPF:

$$I(t) = A(t) \cos [2\pi fct + \phi(t)] \times \cos [2\pi fct + \Delta\theta(t)]$$

$$= (A(t)/2) \cos (\phi(t) - \Delta\theta(t))$$

$$Q(t) = A(t) \cos [2\pi fct + \phi(t)] \times -\sin [2\pi fct + \Delta\theta(t)]$$

$$= (A(t)/2) \times \cos (\phi(t) - \Delta\theta(t))$$

Thus, adverse influence of the frequency offset appears on the orthogonal demodulation output. By this, the phase of an input signal of the A/D converter is shifted to cause offset

from a desired sampling timing.

Examples of the prior art of this kind have been disclosed in (1) Japanese Unexamined Patent Publication No. Heisei 8-223132, (2) Japanese Unexamined Patent Publication No. Heisei 10-260653 and (3) Japanese Patent No. 2570126 (hereinafter referred to as prior art 1 to 3.

The prior art 1 is designed to insert a pilot signal to the transmission signal, derive a frequency offset Δk and a synchronization offset δ of the sampling timing on the basis of the transmission frequency k of the pilot signal and the reception frequency k', and control the sampling period and a transmission frequency of a frequency converter so as to reduce the foregoing offsets to zero.

The prior art 2 is designed for controlling a delay amount of the sampling clock and for controlling the phase of the sampling clock of the input video signal S1 to the phase adapted for the input video signal S1.

The prior art 3 is designed for extracting a clock signal component from a demodulation base band signal and outputting a signal synchronized with the clock signal component as a sampling clock.

As set forth above, in the foregoing prior arts 1 to 3, the ploblem that the phase of the input signal of the A/D converter is shifted to cause offset from the desired sampling timing is solved by controlling the sampling frequency.

However, when the sampling frequency in the A/D converter is increased in order to reduce error in symbol judgment, increasing of power consumption is caused in proportion to increasing of the frequency.

Increasing of power consumption causes significant problem in the equipment desired to be compact and to be used for a long period, such as a communication terminal, e.g. current cellular phone terminal.

SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide a demodulation circuit and a demodulation method which can optimize sampling timing with achieving reduction of power consumption.

According to the first aspect of the present invention, a demodulation circuit for demodulating a digital transmission signal, wherein

a preliminarily known signal is inserted in the digital transmission signal upon transmission,

the demodulation circuit comprises:

A/D converting means for performing A/D conversion of a base band signal obtained by demodulation of the digital transmission signal; and

phase shifting means for causing phase shift of one of the digital transmission signal and the base band signal on the basis of the known signal after digital conversion by the A/D converting means and the known signal upon transmission.

According to the second aspect of the present invention, a modulation circuit for modulating a digital signal comprises:

known signal inserting means for inserting a preliminarily known signal to the digital signal; and

modulating means for modulating the digital signal after insertion of the known signal.

According to the third aspect of the present invention, a demodulation method for demodulating a digital transmission signal, wherein

a preliminarily known signal is inserted in the digital transmission signal upon transmission,

the demodulation method comprising:

first step of performing A/D conversion of a base band signal obtained by demodulation of the digital transmission signal; and

second step causing phase shift of one of the digital transmission signal and the base band signal on the basis of the known signal after digital conversion in the first step and the known signal upon transmission.

According to the fourth aspect of the present invention, a modulation circuit for modulating a digital signal comprising:

fifth step of inserting a preliminarily known signal to the digital signal; and

sixth step of modulating the digital signal after insertion of the known signal.

BREIF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given hereinafter with reference to the accompanying drawings of the preferred embodiment of the present invention, which, however, should not be taken to be limitative to the present invention, but are for explanation and understanding only.

In the drawings:

Fig. 1 is a block diagram showing a construction of the first embodiment of a demodulation circuit according to the present invention;

Fig. 2 is a block diagram showing a construction of the second embodiment of a demodulation circuit according to the present invention;

Fig. 3 is an explanatory illustration showing an insertion method of a known signal to be inserted in a transmission data;

Fig. 4 is an explanatory illustration showing an insertion method of a known signal to be inserted in a transmission data;

Fig. 5 is a flowchart showing a comparison method in a comparator 15;

Fig. 6 is an illustration showing a relationship between a phase amount to be output from a phase shift control portion 14 and a correlation amount;

Fig. 7 is a block diagram showing a construction of the third embodiment of a demodulation circuit according to

the present invention;

Fig. 8 is a flowchart showing operation of the first embodiment of the demodulation circuit;

Fig. 9 is a flowchart showing operation of the second embodiment of the demodulation circuit;

Fig. 10 is a flowchart showing operation of the second embodiment of the demodulation circuit;

Fig. 11 is a flowchart showing operation of the third embodiment of the demodulation circuit;

Fig. 12 is a schematic block diagram showing the fourth embodiment of a modulation circuit;

Fig. 13 is a schematic block diagram showing the fifth embodiment of the modulation circuit;

Fig. 14 is a flowchart showing operation of the fourth embodiment of the demodulation circuit; and

Fig. 15 is a flowchart showing operation of the fifth embodiment of the demodulation circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention will be discussed hereinafter in detail in terms of the preferred embodiment of the present invention with reference to the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to those skilled in the art that the present invention may be practiced without these specific details. In other instance, well-known structure are not shown in detail in order to avoid

unnecessary obscurity of the present invention.

It should be noted that a digital transmission signal in the present invention is a signal which is orthogonally modulated.

At first, the first embodiment of a demodulation circuit according to the present invention will be discussed. Fig. 1 is a block diagram of the first embodiment of the demodulation circuit 51.

Referring to Fig. 1, the demodulation circuit 51 includes an antenna 21, a high frequency receiving portion 1 receiving a signal from the antenna 21, an orthogonal demodulator (ODEM) 2, phase shifters 3 and 4 for phase shifting a signal from the orthogonal demodulator 2, low pass filters (LPF) 5 and 6 for passing lower band of the signals from the phase shifters 3 and 4, A/D converters 7 and 8 performing A/D conversion of signals from the low pass filters 5 and 6, digital filters 9 and 10 passing predetermined frequencies of the signals from the A/D converters 7 and 8, a symbol judgment portion 11 performing symbol judgment of the signals from the digital filters 9 and 10, parallel/serial (P/S) converter 12 for converting a parallel signal from the symbol judgment portion 11 to a serial signal, a reception data processing portion 13 for performing reception data processing of the signal from the parallel/serial (P/S) converter 12, a phase shift control portion 14 for performing phase shift control of the signal from the reception data processing portion 13, a storage

portion 16 preliminarily storing a known signal upon transmission, and a comparing portion 15 extracting a known signal from the parallel signal from the symbol judgment portion 11 and comparing the extracted known signal with the known signal upon transmission stored in the storage portion 16.

While detail will be discussed later, the known signal is inserted in a transmission data in the present invention. A result of comparison of a result of symbol judgment of the known signal by the symbol judgment portion 11 and the known signal for transmission is input to the phase signal control portion 14 for shifting phases of the signals to be input to the A/D converters 7 and 8 on the basis of result of comparison.

Next, operation of the demodulation circuit 51 constructed as set forth above, will be discussed with reference to Fig. 8. A received wave is input to the orthogonal demodulator 2 via the antenna 21 and the high frequency receiving portion 1. A base band signal of the received wave is extracted in the orthogonal demodulator 2 (S1). Next, I component and Q component as output of the orthogonal demodulator 2 respectively pass phase shifters 3 and 4 and unnecessary components are removed from the I component and the Q component by the low pass filters 5 and 6. The I component and Q component removed unnecessary components are subject to A/D conversion by the A/D converters 7 and 8. A/D converted outputs are wave-shaped

by the digital filters 9 and 10 in order to avoid intersymbol interference, and then input to the symbol judgment portion 11 (S2). A symbol judgment output is converted into a serial data by the P/S (parallel/serial) converter 12. Then, a desired demodulated output signal is taken out from the received data processing portion 13.

On the other hand, the comparator 15 takes out the known signal from the output of the symbol judgment portion 11. The known signal compares the known signal stored in the storage portion 16 (S3). The phase shift control portion 14 causes the phase shifters 3 and 4 phase shifting on the basis of the result of comparison by the comparing portion 15 (S4).

Next, insertion method the known signal inserted in the transmission data will be discussed. Figs. 3 and 4 are diagrammatic explanatory illustration showing the insertion method of the known signal inserted in the transmission data. There are two kinds of methods for inserting the known signal in the transmission data. Fig. 3 shows the first method and Fig. 4 shows the second method.

At first, first known signal insertion method will be discussed. Referring to Fig. 3, the first known signal insertion method multiplexes a known data symbol 31 and an information data symbol 32 in time. A time multiplexed digital transmission signal is input to the orthogonal demodulator 2.

Next, discussion will be given for the second known signal insertion method. Referring to Fig. 4, the

information data symbol 32 is assigned to the I channel, and the known data symbol 31 is assigned to the Q channel. These I channel and Q channel are multiplexed. It is also possible to assign the information data symbol 32 to the Q channel and the known data symbol 31 to the I channel.

Next, comparing method in the comparing portion 15 will be discussed. Fig. 5 is a flowchart showing a comparison method in the comparing portion 15. Referring to Fig. 5, the comparison result is output from the comparator 15. Then, the phase shift control portion 14 outputs phase shifting amount to the phase shifters 3 and 4 on the basis of results of comparison (S11). The phase shifters 3 and 4 cause phase shift of the base band signal in the extent corresponding to the phase shifting amount. After phase shifting, the base band signal is input to the A/D converters 7 and 8 via the low pass filters 5 and 6 for A/D conversion (S12).

The signals after A/D conversion are input to the symbol judgment portion 11 via the digital filters 9 and 10 for symbol judgment. The comparing portion 15 takes out the known signal from the symbol judgment portion 11 to compare with the taken out known signal with a known signal upon transmission stored in the storage portion 16 (S13). The result of comparison is stored in a not shown storage portion in the phase shift control portion 14.

The comparing portion 15 is checked whether comparison is repeated for N (N is integer greater than or equal to two) times (S14). If number of times of comparison is less than

N times, the processes at steps S11 to S13 are repeated. Once, number of times of comparison reaches N times, an optimal phase shifting amount is detected on the basis of the N in number of results of comparison (S15). The optimal phase shifting amount is also stored in the not shown storage portion in the phase shift control portion 14.

Next, check is performed whether detection of the optimal phase shifting amount is performed for M (M is positive integer) times (S16). If M times is not reached, the process steps S11 to S15 are repeated. Once M times is reached, an average of M in number of the optimal phase shifting amounts is detected (S17). Then, the phase shift control portion 14 controls the phase shifters 3 and 4 with the average of the M in number of optimal phase shifting amount (S18).

Next, discussion will be given what is "optimal phase shifting amount". The comparing portion 15 derives a correlated value of a known data string upon transmission and a known data string upon reception as the result of comparison.

Now, as one example of the known data string upon transmission is assumed as "+1+1-1+1-1-1+1+1" (8 bit data string). When this is received on the reception side, if the result of symbol judgment in the symbol judgment portion 11 is "+1+1-1+1-1-1+1+1" the same as the known data string upon transmission, the comparing portion 15 obtains "1" as the correlated value normalized by number of data.

On the other hand, if the result of judgment by the symbol judgment portion 11 is "-1+1-1+1-1-1+1-1" (error in two bits), the correlated value of 4/8 = 0.5 can be obtained. Namely, the correlated value for the most recent phase shifting amount is 0.5. Namely, the correlated value closer to 1 represents lesser error.

Next, discussion will be given why the correlated value becomes 0.5 at two bit error. If data upon transmission is "+1" and data upon reception is also "+1", product of these also becomes "+1". Similarly, if data upon transmission is "-1" and data upon reception is also "-1", product of these also becomes "+1". Namely, when the product is "+1", judgment can be made that bit error is not caused.

On the other hand, if data upon transmission is "+1" and data upon reception is also "-1", product of these also becomes "-1". Similarly, if data upon transmission is "-1" and data upon reception is also "+1", product of these also becomes "-1". Namely, when the product is "-1", judgment can be made that bit error is caused.

Accordingly, when bit error is caused at two bits, two products of "-1" appear. In this since correct bits are six bits (+6), error bits are two (-2) and overall bit number is eight bits, 6 - 2 = 4 is established. 4 is a numerator of the foregoing correlation value, and 8 becomes denominator of the foregoing correlated value. Similar discussion will be applicable for bit errors other than two bits.

A relationship between the phase amount (phase

difference of the sampling timing) output from the phase shift control portion 14 and the correlated value is shown Fig. 6. Fig. 6 shows the case where the correlated value for the phase difference $\theta 1$ is r1, ... the correlated value for the phase difference θN is rN.

At step S15, the maximum value of the correlated values r1 to rN can be derived. The phase difference with respect to the maximum amount is taken as the optimal phase shifting amount.

Next, the second embodiment of the demodulation circuit will be discussed. Fig. 2 is a block diagram showing the construction of the second embodiment of the demodulation circuit. The second embodiment is directed to the demodulation circuit 52. It should be noted that like components to those in the first embodiment will be identified by like reference numerals to omit discussion therefor in order to avoid redundant discussion to keep the disclosure simple enough to facilitate clear understanding of the present invention.

Referring to Fig. 2, a point where the second embodiment is differentiated from the first embodiment is that the comparing portion 17 is connected to an output side of the P/S converter 12.

Figs. 9 and 10 are flowcharts showing operation of the second embodiment of the demodulation circuit. Process steps common to the flowchart of the first embodiment will

be identified by like step numbers to omit discussion therefor in order to avoid redundant discussion to keep the disclosure simple enough to facilitate clear understanding of the present invention. Next, operation of the demodulation circuit 52 will be discussed with reference to Figs. 9 and 10.

The A/D conversion output is transmitted to the symbol judgment portion 11 to be judged the symbol. Thereafter, the result of judgment is transmitted to the P/S converter 12 to be converted into the serial data from the parallel data (S5). Next, the comparing portion 17 takes out the known data from data converted into the serial data for comparing with the known data upon transmission stored in the storage portion 16 (S3).

On the other hand, data converted into serial data in parallel to step S3 is transmitted to the reception data processing portion 13 . Then, the known signal is removed (S6) for outputting only information data. Other operation is similar to those of the first embodiment.

It should be noted that while the comparing portion 17 and the storage portion 16 are provided separately from the reception data processing portion 13, these components may be integrated as a reception data processing portion 18.

Next, discussion will be given for the third embodiment. Fig. 7 is a block diagram showing the third embodiment of the demodulation circuit according to the present invention. The third embodiment is directed to the demodulation circuit

53. It should be noted that like components to those in the first and second embodiments will be identified by like reference numerals to omit discussion therefor in order to avoid redundant discussion to keep the disclosure simple enough to facilitate clear understanding of the present invention.

Referring to Fig. 7, the point of the third embodiment different from the first and second embodiments is that a phase shifter 35 is connected between the high frequency receiving portion 1 and the orthogonal demodulator 2. With this, the phase shifter 35 becomes sufficient.

Fig. 11 is a flowchart showing the operation of the third embodiment. Next, operation of the third embodiment will be discussed with reference to Fig. 11. At first, discussion will be given for operation with taking the first embodiment as base. Referring to Fig. 11 together with Fig. 8, the known signals are compared by the comparing portion 15 (S3). Thereafter, the phase shift control portion 14 outputs a phase shifting amount to the phase shifter 35 on the basis of the result of comparison to cause the phase shifter 35 to cause phase shifting of the digital transmission signal as output of the high frequency receiving portion 1 (S7).

Next, discussion will be given with taking the operation of the second embodiment as base. Referring to Fig. 11 together with Fig. 9, the known signals are compared by the comparing portion 15 (S3). Thereafter, the phase shift

control portion 14 outputs a phase shifting amount to the phase shifter 35 on the basis of the result of comparison to cause the phase shifter 35 to cause phase shifting of the digital transmission signal as output of the high frequency receiving portion 1 (S7).

Next, discussion will be given for the fourth embodiment. Fig. 12 is a block diagram of a modulation circuit according to the present invention. The fourth embodiment is directed to the modulation circuit 61. Referring to Fig. 12, the modulation circuit 61 includes a time multiplexing portion 62, a serial/parallel (S/P) converter 63 and an orthogonal modulating portion 64 (64a and 64b).

Fig. 14 is a flowchart showing operation of the fourth embodiment of the present invention, Operation of the modulation circuit 61 will be discussed with reference to Fig. 14. At first, an information data 30 is divided into a plurality of information data 32 by the time multiplexing portion 62 and the information data 32 is time multiplexed with the known data 31 (S21). Namely, information data 32 and the known data 31 are alternately output in time series. Next, the time multiplexed data is converted into the parallel data by the S/P converter 63. Thereafter, respective data are orthogonally modulated by the orthogonal modulating portions 64a and 64b (S22). Then, the digital transmission data orthogonally modulated is received by the demodulators 51 to 53 on reception side.

Next, discussion will be given for the fifth embodiment of the modulation circuit. Fig. 13 is a block diagram of the fifth embodiment. The fifth embodiment is directed to a modulation circuit 65. It should be noted that like components to those in the fourth embodiment (Fig. 12) will be identified by like reference numerals to omit discussion therefor in order to avoid redundant discussion to keep the disclosure simple enough to facilitate clear understanding of the present invention.

Referring to Fig. 13, the modulation circuit 65 is constructed with including the orthogonal modulating portion 64a and 64b.

Fig. 15 is a flowchart showing the operation of the fifth embodiment of the modulation circuit. Operation of the modulation circuit 65 will be discussed with reference to Fig. 15. At first, the information data 32 is assigned to the I channel and the known data 31 is assigned to the Q channel (S31). Next, in the orthogonal modulating portions 64a and 64b, the information data 32 and the known data 31 are orthogonally modulated (S32). Then, the orthogonally modulated digital transmission data is received by the demodulators 51 to 53 on reception side.

With the invention set forth above, in the demodulation circuit for demodulating the digital signal, the preliminarily known signal is inserted to the digital transmission signal upon transmission, and the demodulation circuit includes the A/D converting means for performing A/D

conversion of the base band signal obtained by demodulation of the digital transmission signal, and the phase shifting means for causing phase shift of the digital transmission signal or the base band signal on the basis of the known signal after digital conversion by the A/D converting means and the known signal for transmission so as to enable optimization of sampling timing with achieving reduction of power consumption.

Also, with the present invention, the modulation circuit for modulating the digital signal includes the known signal inserting means for inserting the preliminarily known signal to the digital signal and the modulating means for modulating the digital signal after insertion of the known signal. Thus the effect set forth above can be achieved.

Furthermore, with the present invention, in the demodulation method for demodulating the digital signal, the preliminarily known signal is inserted to the digital transmission signal upon transmission, and the demodulation circuit includes a step of performing A/D conversion of the base band signal obtained by demodulation of the digital transmission signal, and a step of causing phase shift of the digital transmission signal or the base band signal on the basis of the known signal after digital conversion in the A/D conversion step and the known signal for transmission so as to enable optimization of sampling timing with achieving reduction of power consumption.

Also, with the present invention, the modulation

method for modulating the digital signal includes the a step inserting the preliminarily known signal to the digital signal and a step of modulating the digital signal after insertion of the known signal. Thus the effect set forth above can be achieved.

Namely, according to the present invention, since the sampling timing can be optimized with maintaining the sampling frequency low by shifting the phase of the input signal of the A/D converter, the power consumption which can be increased according to increasing of the sampling frequency, can be lowered.

Furthermore, error in symbol judgment can be reduced to achieve good reception characteristics. This is achieved by capability of maintaining the sampling timing of the A/D converter optimal by the phase shift control portion and the phase shifter.

Although the present invention has been illustrated and described with respect to exemplary embodiments thereof, it should be understood by those skilled in the art that the foregoing and various changes, emission and additions may be made therein and thereto, without departing from the spirit and scope of the present invention. Therefore, the present invention should not be understood as limited to the specific embodiment set out above but to include all possible embodiments which can be embodied within a scope encompassed and equivalent thereof with respect to the feature set out in the appended claims.

WHAT IS CLAIMED IS:

1. A demodulation circuit for demodulating a digital transmission signal, wherein

a preliminarily known signal being inserted in said digital transmission signal upon transmission,

said demodulation circuit comprising:

A/D converting means for performing A/D conversion of a base band signal obtained by demodulation of said digital transmission signal; and

phase shifting means for causing phase shift of one of said digital transmission signal and said base band signal on the basis of said known signal after digital conversion by said A/D converting means and said known signal upon transmission.

2. A demodulation circuit as set forth in claim 1, which further comprises orthogonal demodulating means for performing orthogonal demodulation of said digital transmission signal formed with an orthogonal modulated signal,

said A/D converting means includes two A/D converters for performing A/D conversion of two base band signals demodulated by said orthogonal demodulating means and having demodulated phases mutually offset for right angle,

symbol judgment portion for making judgment of symbols of digital signals converted by said two A/D converters ,

said phase shifting means including comparing portion

for comparing said known signal, for which symbol judgment is performed by said symbol judgment portion with said known signal for transmission, and a phase shifter for causing phase shift of said base band on the basis of a result of comparison by said comparing portion.

3. A demodulation circuit as set forth in claim 1, which further comprises orthogonal demodulating means for performing orthogonal demodulation of said digital transmission signal formed with an orthogonal modulated signal,

said A/D converting means includes two A/D converters for performing A/D conversion of two base band signals demodulated by said orthogonal demodulating means and having demodulated phases mutually offset for right angle,

symbol judgment portion for making judgment of symbols of digital signals converted by said two A/D converters,

said phase shifting means including P/S converter for conversing the digital signal, for which symbol judgment is performed by said symbol judgment portion, comparing portion for comparing said known signal serial converted by said P/S converter with said known signal for transmission and a phase shifter for causing phase shift of said base band on the basis of a result of comparison by said comparing portion.

4. A demodulation circuit as set forth in claim 3, which further comprises reception data processing portion

obtaining an information data by removing said known signal from the signal converted into a serial data by said P/S converter.

5. A demodulation circuit as set forth in claim 2, wherein said phase shifter causes phase shift of said digital transmission signal on the basis of the result of comparison by said comparing portion.

6. A demodulation circuit as set forth in claim 1, wherein said phase shifting means outputs different phase shifting amount for N times, (in which N is an integer greater than or equal to two), for detecting shifting amount to be shifted on the basis of the result of comparison of the known signals for N times with respect to respective phase shifting amounts.

7. A demodulation circuit as set forth in claim 6, wherein said phase shifting means causes phase shift to a phase where a correlation value of said known signal for transmission and said known signal after digital conversion by said A/D converting means becomes the highest.

8. A demodulation circuit as set forth in claim 6, wherein said phase shifting means repeats a process for detecting phase amount to be shifted based on the result of comparison for N times for M times, in which M is positive integer to

take an average value of optimal phase shifting amount for M times as a final optimal phase shifting amount.

9. A demodulation circuit as set forth in claim 1, wherein said digital transmission signal is a signal, in which said information data and said known signal are time multiplexed.

10. A demodulation circuit as set forth in claim 1, wherein said digital transmission signal has two base band signals having phases mutually shifted for 90° , in which an information data is assigned for one of said base band signals and said known signal is assigned to the other base band signal.

11. A modulation circuit for modulating a digital signal comprising:

known signal inserting means for inserting a preliminarily known signal to said digital signal; and

modulating means for modulating the digital signal after insertion of said known signal.

12. A modulation circuit as set forth in claim 11, wherein said modulating means is an orthogonal modulator.

13. A modulation circuit as set forth in claim 11, wherein said known signal inserting means inserts said known signal to said digital signal in time multiplexing.

14. A modulation circuit as set forth in claim 11, wherein said known signal inserting means assigns information data to one of two digital signals which are modulated to have phases mutually shifted for 90° and said known signal to the other digital signal.

15. A demodulation method for demodulating a digital transmission signal, wherein

a preliminarily known signal being inserted in said digital transmission signal upon transmission,

said demodulation method comprising:

first step of performing A/D conversion of a base band signal obtained by demodulation of said digital transmission signal; and

second step causing phase shift of one of said digital transmission signal and said base band signal on the basis of said known signal after digital conversion in said first step and said known signal upon transmission.

16. A demodulation method as set forth in claim 15, which further comprises third step of performing orthogonal demodulation of said digital transmission signal formed with an orthogonal modulated signal,

said first step includes first sub-step of performing A/D conversion of two base band signals demodulated by said third step and having demodulated phases mutually offset for

90° , and making judgment of symbols of digital signals converted by said two A/D converters ,

said second step including second sub-step of comparing said known signal, for which symbol judgment is performed by said first sub-step with said known signal for transmission, and third sub-step of causing phase shift of said base band on the basis of a result of comparison by said second sub-step.

17. A demodulation method as set forth in claim 15, which further comprises third step of performing orthogonal demodulation of said digital transmission signal formed with an orthogonal modulated signal,

said first step includes first sub-step of performing A/D conversion of two base band signals demodulated by said third step and having demodulated phases mutually offset for 90° , and making judgment of symbols of digital signals converted by said two A/D converters ,

said second step including fourth sub-step conversing the digital signal, for which symbol judgment is performed by said symbol judgment portion, second sub-step of comparing said known signal serial converted by said fourth sub-step with said known signal for transmission and third sub-step of causing phase shift of said base band on the basis of a result of comparison by said fifth sub-step.

18. A demodulation method as set forth in claim 17, which further comprises fourth step of obtaining an information data by removing said known signal from the signal converted into a serial data by said fourth sub-step.

19. A demodulation method as set forth in claim 16, wherein said second step causes phase shift of said digital transmission signal on the basis of the result of comparison by said second sub-step.

20. A demodulation method as set forth in claim 15, wherein said second step outputs different phase shifting amount for N times, (in which N is an integer greater than or equal to two), for detecting shifting amount to be shifted on the basis of the result of comparison of the known signals for N times with respect to respective phase shifting amounts.

21. A demodulation method as set forth in claim 20, wherein said second step causes phase shift to a phase where a correlation value of said known signal for transmission and said known signal after digital conversion in said first step becomes the highest.

22. A demodulation method as set forth in claim 20, wherein said second step repeats a process for detecting phase amount to be shifted based on the result of comparison for N times for M times, in which M is positive integer to take an average

value of optimal phase shifting amount for M times as a final optimal phase shifting amount.

23. A demodulation method as set forth in claim 15, wherein said digital transmission signal is a signal, in which said information data and said known signal are time multiplexed.

24. A demodulation method as set forth in claim 15, wherein said digital transmission signal has two base band signals having phases mutually shifted for 90° , in which an information data is assigned for one of said base band signals and said known signal is assigned to the other base band signal.

25. A modulation circuit for modulating a digital signal comprising:

fifth step of inserting a preliminarily known signal to said digital signal; and

sixth step of modulating the digital signal after insertion of said known signal.

26. A modulation method as set forth in claim 25, wherein said modulating means is an orthogonal modulator.

27. A modulation method as set forth in claim 25, wherein said fifth means inserts said known signal to said digital signal in time multiplexing.

28. A modulation method as set forth in claim 25, wherein said fifth step assigns information data to one of two digital signals which are modulated to have phases mutually shifted for 90° and said known signal to the other digital signal.

ABSTRACT OF THE DISCLOSURE

A demodulation circuit and a demodulation method can optimize sampling timing with achieving reduction of power consumption. A preliminarily known signal is inserted in the digital transmission signal upon transmission. The demodulation circuit includes A/D converting means for performing A/D conversion of a base band signal obtained by demodulation of the digital transmission signal, and phase shifting means for causing phase shift of one of the digital transmission signal and the base band signal on the basis of the known signal after digital conversion by the A/D converting means and the known signal upon transmission.

FIG.1

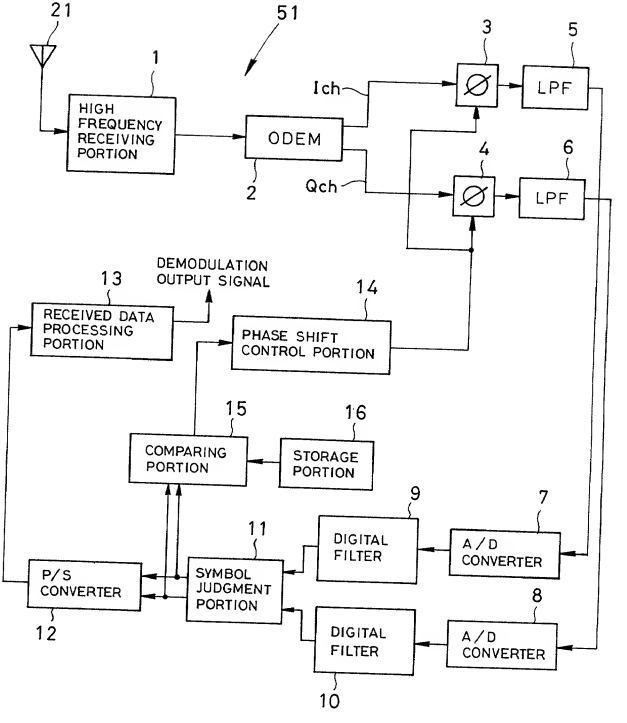

21
51
1
3
5
Ich
HIGH FREQUENCY RECEIVING PORTION
ODEM
LPF
2
Qch
4
6
LPF
DEMODULATION OUTPUT SIGNAL
13
14
RECEIVED DATA PROCESSING PORTION
PHASE SHIFT CONTROL PORTION
15
16
COMPARING PORTION
STORAGE PORTION
9
7
11
DIGITAL FILTER
A/D CONVERTER
P/S CONVERTER
SYMBOL JUDGMENT PORTION
8
DIGITAL FILTER
A/D CONVERTER
12
10

FIG. 2

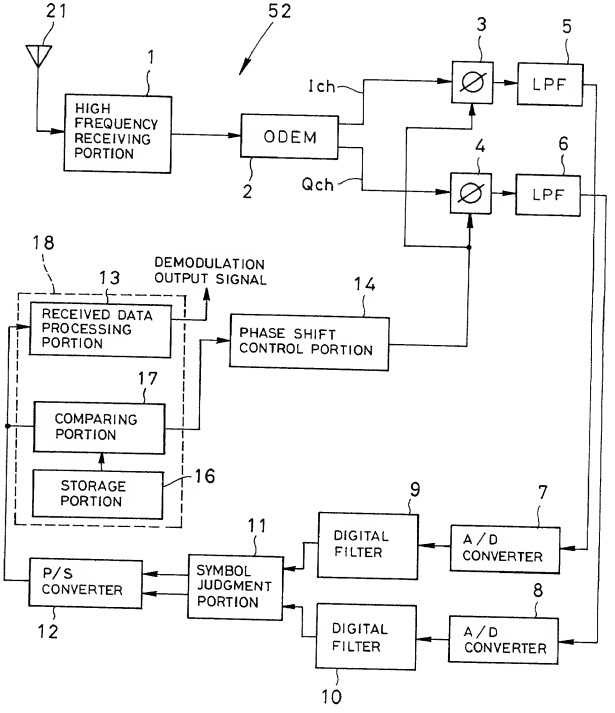

21
52
1
HIGH FREQUENCY RECEIVING PORTION
ODEM
2
Ich
Qch
3
4
5
6
LPF
LPF
18
13
DEMODULATION OUTPUT SIGNAL
RECEIVED DATA PROCESSING PORTION
14
PHASE SHIFT CONTROL PORTION
17
COMPARING PORTION
STORAGE PORTION
16
9
7
11
DIGITAL FILTER
A/D CONVERTER
P/S CONVERTER
SYMBOL JUDGMENT PORTION
8
12
DIGITAL FILTER
A/D CONVERTER
10

FIG. 3

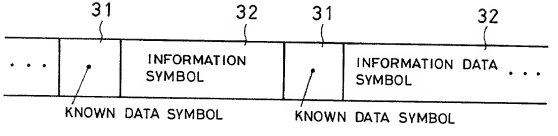

31
32
31
32
INFORMATION SYMBOL
INFORMATION DATA SYMBOL
KNOWN DATA SYMBOL
KNOWN DATA SYMBOL

FIG. 4

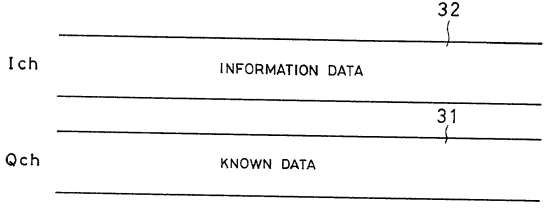

32
Ich
INFORMATION DATA
31
Qch
KNOWN DATA

FIG. 5

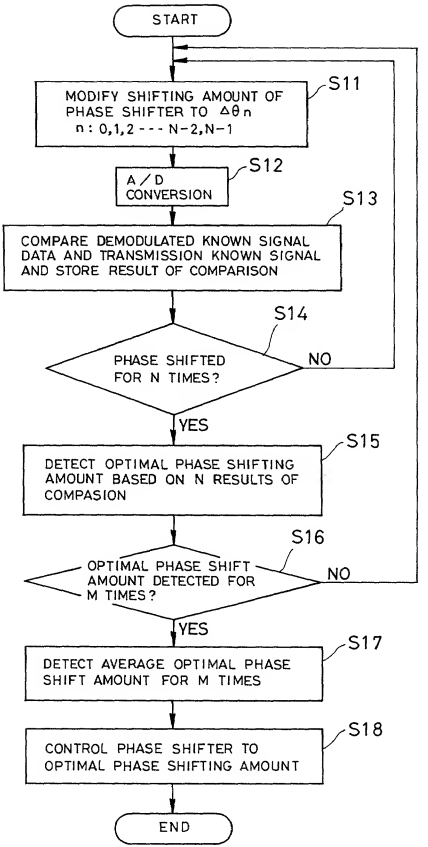

START
MODIFY SHIFTING AMOUNT OF PHASE SHIFTER TO Δθn n : 0,1,2 --- N-2,N-1
S11
A/D CONVERSION
S12
COMPARE DEMODULATED KNOWN SIGNAL DATA AND TRANSMISSION KNOWN SIGNAL AND STORE RESULT OF COMPARISON
S13
PHASE SHIFTED FOR N TIMES?
S14
NO
YES
DETECT OPTIMAL PHASE SHIFTING AMOUNT BASED ON N RESULTS OF COMPASION
S15
OPTIMAL PHASE SHIFT AMOUNT DETECTED FOR M TIMES?
S16
NO
YES
DETECT AVERAGE OPTIMAL PHASE SHIFT AMOUNT FOR M TIMES
S17
CONTROL PHASE SHIFTER TO OPTIMAL PHASE SHIFTING AMOUNT
S18
END

FIG. 6

SAMPLING TIMING PHASE DIFFERENCE	θ1 θ2 θ3 --- θN-2 θN-1 θN
CORRELATION VALUE	r1 r2 r3 --- rN-2 rN-1 rN

FIG. 7

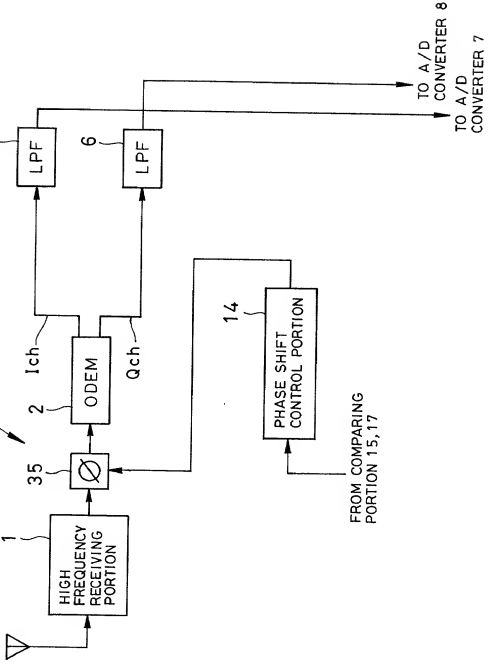

53
1
HIGH FREQUENCY RECEIVING PORTION
35
2
ODEM
Ich
Qch
5
LPF
6
LPF
14
PHASE SHIFT CONTROL PORTION
FROM COMPARING PORTION 15,17
TO A/D CONVERTER 8
TO A/D CONVERTER 7

FIG. 8

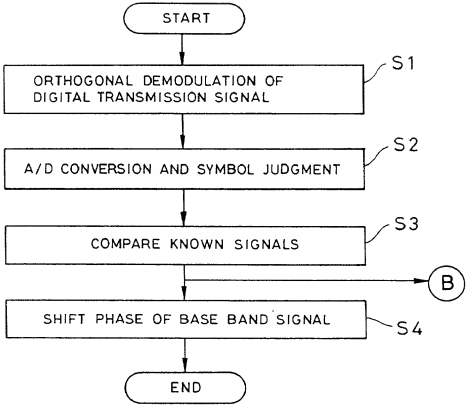

START
ORTHOGONAL DEMODULATION OF DIGITAL TRANSMISSION SIGNAL
S1
A/D CONVERSION AND SYMBOL JUDGMENT
S2
COMPARE KNOWN SIGNALS
S3
B
SHIFT PHASE OF BASE BAND SIGNAL
S4
END

FIG. 9

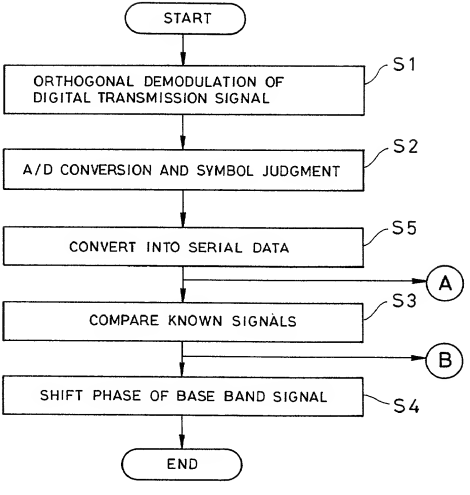

START
ORTHOGONAL DEMODULATION OF DIGITAL TRANSMISSION SIGNAL
S1
A/D CONVERSION AND SYMBOL JUDGMENT
S2
CONVERT INTO SERIAL DATA
S5
A
COMPARE KNOWN SIGNALS
S3
B
SHIFT PHASE OF BASE BAND SIGNAL
S4
END

FIG.10

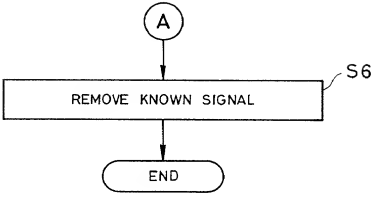

A
S6
REMOVE KNOWN SIGNAL
END

FIG.11

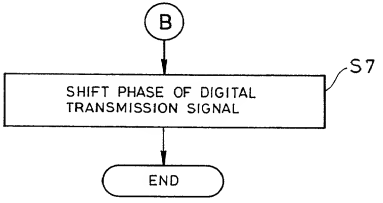

B
S7
SHIFT PHASE OF DIGITAL TRANSMISSION SIGNAL
END

FIG.12

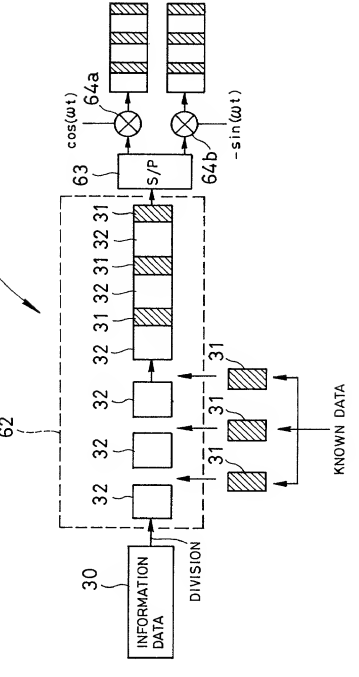

30
INFORMATION DATA
DIVISION
62
61
32
31
KNOWN DATA
63
S/P
64a
64b
cos(ωt)
-sin(ωt)

FIG.13

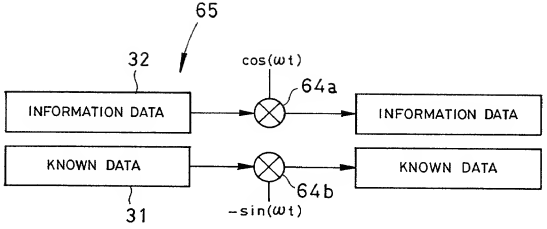

65
32
cos(ωt)
64a
INFORMATION DATA
INFORMATION DATA
KNOWN DATA
KNOWN DATA
64b
31
-sin(ωt)

FIG.14

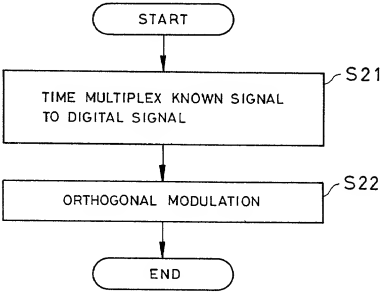
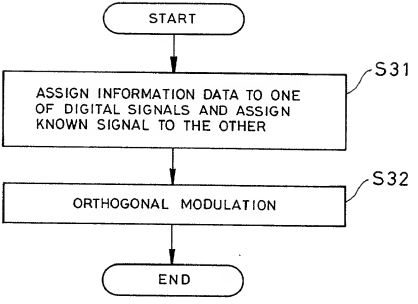

START
TIME MULTIPLEX KNOWN SIGNAL TO DIGITAL SIGNAL
S21
ORTHOGONAL MODULATION
S22
END

FIG.15


START
ASSIGN INFORMATION DATA TO ONE OF DIGITAL SIGNALS AND ASSIGN KNOWN SIGNAL TO THE OTHER
S31
ORTHOGONAL MODULATION
S32
END

Docket No.

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DEMODULATION AND MODULATION CIRCUIT AND DEMODULATION AND MODULATION METHOD -

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
045636/ 1999 (Number)	Japan (Country)	February 24, 1999 (Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Stephen D. Murphy, Reg. No.: 22,002

Paul J. Esatto, Reg. No.: 30,749

William C. Roch, Reg. No.: 24,972

Mark J. Cohen, Reg. No.: 32,211

Frank S. DiGiglio, Reg. No.: 31,346

Donald T. Black, Reg. No.: 27,999

Send Correspondence to: **Paul J. Esatto, Jr.**
Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530

Direct Telephone Calls to: *(name and telephone number)*
Paul J. Esatto, Jr. (516) 742-4343

Full name of sole or first inventor	KOICHI TAMURA
Sole or first inventor's signature	Koichi Tamura — Date: 1, February, 2000
Residence	Tokyo, Japan
Citizenship	Japan
Post Office Address	c/o NEC Corporation 7-1, Shiba 5-chome, Minato-ku, Tokyo,Japan

Full name of second inventor, if any	
Second inventor's signature	Date
Residence	
Citizenship	
Post Office Address	